AIC HW4

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|  |  |  |  |
| --- | --- | --- | --- |
|  | Fig.(a) | Fig.(b) | Fig.(c) |
| Av(dB) | 17.9287 | 0.06003 | 18.0703 |
| 3-dB bandwidth (Hz) | 90.622M | 229.905M | 117.372M |

## Problem 1

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Fig. 1: Low-Frequency Gain .measure Result

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Fig. 2: -3dB Gain

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Fig. 3: Circuit (a) -3dB Freq.

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Fig. 4: Circuit (b) -3dB Freq.

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Fig. 5: Circuit (c) -3dB Freq.

## Problem 1 Code

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

4. .lib "~/U18\_HSPICE\_Model/mm180\_reg18\_v124.lib" tt

5. .TEMP 25

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10.

11. .option post

12. .AC DEC 100 1n 100G

13.

14. \*\*\*-----------------------\*\*\*

15. \*\*\*      parameters       \*\*\*

16. \*\*\*-----------------------\*\*\*

17. .global VDD GND

18. \*\*\*-----------------------\*\*\*

19. \*\*\*       measure         \*\*\*

20. \*\*\*-----------------------\*\*\*

21. .measure ac Gain\_a      FIND V(VOUT\_a) at=10000Hz

22. .measure ac Gain\_b      FIND V(VOUT\_b) at=10000Hz

23. .measure ac Gain\_c      FIND V(VOUT\_c) at=10000Hz

24.

25. \*\*\*-----------------------\*\*\*

26. \*\*\*      power/input      \*\*\*

27. \*\*\*-----------------------\*\*\*

28. Vsupply VDD GND 1.8V

29.

30. \*\*\*-----------------------\*\*\*

31. \*\*\*        circuit        \*\*\*

32. \*\*\*-----------------------\*\*\*

33.

34. Xa  VIN\_a   VOUT\_a  CKT\_A

35. Xb  VIN\_b   VOUT\_b  CKT\_B

36. Xc  VIN\_c   VOUT\_c  CKT\_C

37.

38. .subckt CKT\_A   VIN     VOUT

39. RD  VDD     VOUT   15k

40. RS  VIN     Gate   10k

41. MN  VOUT    Gate   GND     GND      n\_18\_mm w=13u l=1.3u

42. C1  VOUT    GND    0.02p

43. V1  VIN     GND    DC      0.6V     AC  1

44. .ends

45.

46. .subckt CKT\_B   VIN     VOUT

47. RD  VDD     VOUT   15k

48. RS  VIN     Source 10k

49. MN  VOUT    Vb     Source  GND      n\_18\_mm w=13u l=1.3u

50. C1  VOUT    GND    0.02p

51. V1  VIN     GND    DC      0.3V     AC  1

52. V2  Vb      GND    DC      0.9V

53. .ends

54.

55. .subckt CKT\_C   VIN     VOUT

56. RD  VDD     VOUT   15k

57. RS  VIN     G1     10k

58. MN2 VOUT    Vb     VX      VX      n\_18\_mm w=13u l=1.3u

59. MN1 VX      G1     GND     GND     n\_18\_mm w=13u l=1.3u

60. C1  VOUT    GND    0.02p

61. V1  VIN     GND    DC      0.6V     AC  1

62. V3  Vb      GND    0.9V

63. .ends

64.

65. .end

## Problem 2:

Compare both low-frequency voltage gain Av and 3-dB bandwidth between these two amplifiers in Figs. (a) and (b). Please explain the reasons why they are larger or smaller.

Circuit (a) is a CS amplifier. Because the gate oxide is SiO2(basically glass), its input resistance looking into the gate is very high. On the other hand, circuit (b) is a CG amplifier, the input resistance looking into the source is given by 1/gm. 1/gm is typically only 1~2kΩ. After voltage division with Rs (10kΩ), the input voltage is significantly reduced to less than 20% its original value. This is why even though circuit (a) & (b) have identical output resistance, but (b) has a lower gain. This low input resistance problem can be resolved by using a cascode amplifier, as shown in circuit (c).

While CS amplifiers have the advantage of high input resistance, they have the problem of small bandwidth due to Miller effect. Due to this, the input capacitance is greatly increased, as shown by the following equation:

Cin ​≈ Cgd​ × ( 1 + ∣Av​∣ )

CG amplifiers do not experience Miller effect, so they have a larger gain bandwidth. As shown in problem 1, the CS amplifier of circuit (a) only has a bandwidth of 90.1MHz, while the CG amplifier of circuit (b) has a bandwidth of 231MHz. We can combine the best of both worlds: high input resistance & large bandwidth by using a cascode amplifier, like the one in circuit (c).

## Problem 3:

Compare both output noise voltage and input-referred noise between these two amplifiers in Figs. (a) and (c). Please describe the results you observed and explain whether you think MN2 in Fig. (c) has a significant impact on the total output noise. If not, please explain the reason for your assessment.

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Fig. 6: Circuit (a) innoise & outnoise 1 ~ 150MHz

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Fig. 7: Circuit (a) Input-referred Noise

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Fig. 8: Circuit (c) innoise & outnoise 1 ~ 150MHz

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Fig. 9: Circuit (c) Input-referred Noise

MN2 of circuit(c) has very small impact on the total output noise at low frequencies. We can use the following equivalent circuit to analyze this:

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Fig. 10: Equivalent Circuit for M2 Input-referred Noise

In this circuit, the input-referred noise of M2 passes through a source-degenerated CS configuration, whose Gm is given by:

The equation indicates that the gain seen from the M2’s gate to M2’s drain is small if Rx is large. In order to prove this through simulation, I modified my code to run an AC analysis from M2’s gate to M2’s drain. Notice that the gain at low frequency is quite small. However, the gain begins to increase past 10MHz. This is due to the capacitance at node X. At high frequencies, the gain from M2’s gate to M2’s drain is given by:

Therefore, M2 starts contributing more to the total output noise as the frequency increases.

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Fig. 11: Circuit (c) innoise & outnoise 1 ~ 150MHz from M2’s gate to M2’s drain

## Problem 3 Code:

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

4. .lib "~/U18\_HSPICE\_Model/mm180\_reg18\_v124.lib" tt

5. .TEMP 25

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10.

11. .option post

12. .ac    DEC  100 1 150Meg

13. .noise V(VOUT\_a)   VA  1

14.

15. \*\*\*-----------------------\*\*\*

16. \*\*\*      parameters       \*\*\*

17. \*\*\*-----------------------\*\*\*

18. .global VDD GND

19. \*\*\*-----------------------\*\*\*

20. \*\*\*       measure         \*\*\*

21. \*\*\*-----------------------\*\*\*

22.

23. \*\*\*-----------------------\*\*\*

24. \*\*\*      power/input      \*\*\*

25. \*\*\*-----------------------\*\*\*

26. Vsupply VDD GND 1.8V

27. VA  VIN\_a     GND    DC      0.6V     AC  1

28. VC  VIN\_c     GND    DC      0.6V     AC  1

29.

30. \*\*\*-----------------------\*\*\*

31. \*\*\*        circuit        \*\*\*

32. \*\*\*-----------------------\*\*\*

33. Xa  VIN\_a   VOUT\_a  CKT\_A

34. Xc  VIN\_c   VOUT\_c  CKT\_C

35.

36. .subckt CKT\_A   VIN     VOUT

37. RD  VDD     VOUT   15k

38. RS  VIN     Gate   10k

39. MN  VOUT    Gate   GND     GND      n\_18\_mm w=13u l=1.3u

40. C1  VOUT    GND    0.02p

41. \*V1  VIN     GND    DC      0.6V     AC  1

42. .ends

43.

44. .subckt CKT\_B   VIN     VOUT

45. RD  VDD     VOUT   15k

46. RS  VIN     Source 10k

47. MN  VOUT    Vb     Source  GND      n\_18\_mm w=13u l=1.3u

48. C1  VOUT    GND    0.02p

49. V1  VIN     GND    DC      0.3V     AC  1

50. V2  Vb      GND    DC      0.9V

51. .ends

52.

53. .subckt CKT\_C   VIN     VOUT

54. RD  VDD     VOUT   15k

55. RS  VIN     G1     10k

56. MN2 VOUT    Vb     VX      VX      n\_18\_mm w=13u l=1.3u

57. MN1 VX      G1     GND     GND     n\_18\_mm w=13u l=1.3u

58. C1  VOUT    GND    0.02p

59. V3  Vb      GND    0.9V

60. .ends

61.

62. .alter

63. .noise V(VOUT\_c)   VC  1

64.

65. .end

66.